Lab 4

ECE 3300 LAB

SECTION 02

Instructor: Mohamed Aly

October 4, 2021

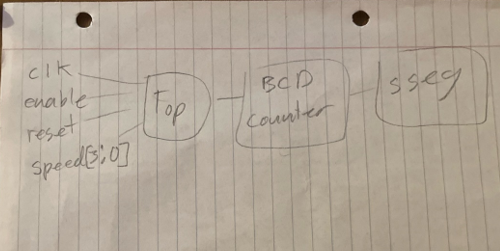
Group I

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| --- | --- | --- |
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**Abstract**

Purpose of the experiment was to loop from 0-9 on the Arty 7 FPGA board. Task was to create 4x16 decoder, BCD counter and segment display. One button would be used to reset the clock speed. Decoder was created using structural modeling. From there, the switches would be used to change how quickly the numbers would be displayed.

**Theory: Sketch of Design**



**Area/Resources Information**

Elaborated Design

Diagram, schematic

Description automatically generated

**Power Usage**

**Graphical user interface, text, application

Description automatically generated**

**Post-Implementation Resource Utilization**

